8.1 A 232-Channel Visual Prosthesis ASIC with Production-Compliant Safety and Testability

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Functional electrical stimulation of retinal tissue with bipolar current pulses has been proven to restore basic visual reception [1-3]. But, in addition to producing a large number of stimulation sites and basic functionality, test and safety issues have to be solved to be ready for production. We describe here a retinal stimulator in 0.35µm high-voltage (HV) CMOS with 232 digitally programmable stimulation channels. The unique features of the ASIC are architectural innovations, its flexibility and programmability, the testability and the biological and electrical safety features. These features allow its usage for extensive tests and chronic implants. The system is shown in Fig. 8.1.1 and the stimulator micrograph is given in Fig. 8.1.2. There are globally dedicated and locally distributed functions [2].

The global functions manage the communication, power supply and stimulation control; simplified schematics are given in Fig. 8.1.3: a 32b Poly fuse Programmable ROM (PPROM) block contains a 24b ID word and 8b for analog tuning. Power is transmitted wirelessly at 13.56MHz and 3 supplies are generated from 2 separate off-chip power coils with 2 rectifiers: $V_{Low} \approx 3.5$ to 5V, $V_{DDP} > 20$V for stimulation and a middle tap connection $V_{CM} \approx V_{DDP}/2$ as stimulator common ground. Two supply regulators are realized: a series regulator receives a startup voltage over a diode network. Therewith, the supply for low-voltage electronics V_{DDA} is pulled above 2V. As soon as the bandgap reference exceeds the startup voltage, it takes over the regulation and $V_{DDA} \approx 3.3$V. The reference is also used to resistively generate an on-chip reference current. Since both the bandgap voltage and the reference current vary over process, they are tuned on chip with a resistor array using 4b of the PPROM during production test. The high supply is controlled by a shunt regulator to 22.5V. Therefore, the middle tap is connected over a bipolar diode string to ground; if V_{CM} becomes high, transistor M_1 in Fig. 8.1.3 is turned on and reduces $V_{DDP} \approx 2V_{CM} \approx 22$V.

The 968kbps Manchester-coded data is optically transmitted to the prosthesis and received by an off-chip photo diode. The signal strength is 2 to 50µA and a strong DC background of 10 to 100µA is expected from ambient light. Therefore, a transimpedance amplifier (TIA) is combined with a DC-suppressing feedback loop, Fig. 8.1.3. In order to avoid a poor PSRR due to the large junction capacitance, the diode is connected between ground and the TIA input.

Incoming stimulation data consists of 16 bits of global data per frame, 16 bits of local data for each addressed electrode and a 16b CRC sum. Global data is either for normal operation or test: both modes allow the choice of 6 biphasic pulse shapes [2], and 6b timing information for a half pulse with a maximum length of 3.3ms. Test operation allows an ADC sampling time specified with 7b, so the maximum time is 6.6ms.

Each packet of local data contains 8 bits of electrode address and 8 bits of amplitude information. The stimulation current is programmed with 5b resolution in 4 ranges with maximum 1mA and DR = 48dB. The maximum number of electrodes in one frame is 116 out of 232, since each 2 electrodes share one digitally programmable stimulation pad cell similar to [2]. Every cell features a local control, a 5b current steering DAC, a HV output current source, an active charge balancer, and a resistive voltage divider with a subsequent T/H. In contrast to [2], each pad cell controls 2 electrodes: since only the HV interfacing transistors are implemented twice, more electrodes can be realized on limited die area. The measured electrode output voltage at one electrode for all adjustable push and pull currents is shown in Fig. 8.1.4, together with the push-pull current mismatch; the latter is <5% for all amplitudes and can be easily removed by the active charge balancer after each stimulation cycle.

During data reception, the digital controller only stores the timing information. For each received 16 bits of local data, one of 232 electrodes is addressed via a row-column decoder, the amplitude data are then digitally distributed and locally stored in the stimulation cells. The controller triggers the biphasic stimulation and afterwards the active charge balancing over a 4b bus. A new stimulation is only started if $V_{DDA} \geq 3$V, the previous stimulation is finished successfully and correct new data are available. Thus, a stimulation protocol is transmitted wirelessly, but complete control of the stimulation is internally performed and its safety concurrently monitored. Measured biphasic output waveforms with charge balancing are shown in Fig. 8.1.5.

The safety of the retinal stimulator is important in several ways: safe ASIC handling must be assured for integrity; safe implant programming and operation need to be guaranteed and testable after implantation, and the bio-electrical interface must not be harmed by electrolysis. Among other measures the internal protocol assures biphasic stimulation and charge balancing are actively controlled at each electrode [2]. In addition, custom ESD protection for safe handling during production test and surgery is implemented at each I/O pad. Another unique feature is the detection of unwanted stimulation currents. Therefore, the current safety controller in Fig. 8.1.6 shorts the counter-electrode and the common V_{CM} only during stimulation. Otherwise a 10kΩ resistor is present showing a significant voltage drop in case of unwanted currents. This voltage drop is detected by the HV window comparator, which consists of a HV Gm stage, 2 low-voltage comparators (±200mV) and which is designed for low offset. A measured current window is shown in Fig. 8.1.7 and the successful generation of a ±20µA window is obvious.

Full production testing of all analog functions as well as a scan chain test are performed. After startup, a unique test electrode (not connected to the tissue) can be activated. It closes a switch between the electrode and ground when addressed for stimulation. This forces a current and charge balancer safety error and enables a test of the critical safety features after implantation.

The back communication is done with pulse-position load modulation for power reasons. Two 1µs pulses are used in each 100µs period in order to generate a 20kbps backchannel, which is used for operational implant information and internal data. Internal data is either the implant ID, an A/D converted sampled electrode potential during test mode, or error states: unwanted current, unfinished charge balancing, CRC error, and others.

The basic current for the global functions is 2mA from 3.3V, 200µA from V_{CM} and 20µA from the high supply V_{DDP}. The bias shunt current can be programmed between 130 and 250µA [4]. Total power consumption is strongly dependent on the protocol. For example, for 3mA of summed stimulation currents (high supply) into 32 electrodes, the overhead current consumption by the local functions can be <1mA from the low supply, and <350µA from the high supply.

The presented stimulator ASIC is ready for implantation and currently under implant assembly. It includes distributed functionality, 232 total/116 independent stimulation channels, production and operational testability as well as unique safety features. It is the first epi-retinal stimulator with this safety, complexity, and this number of electrodes.

References:
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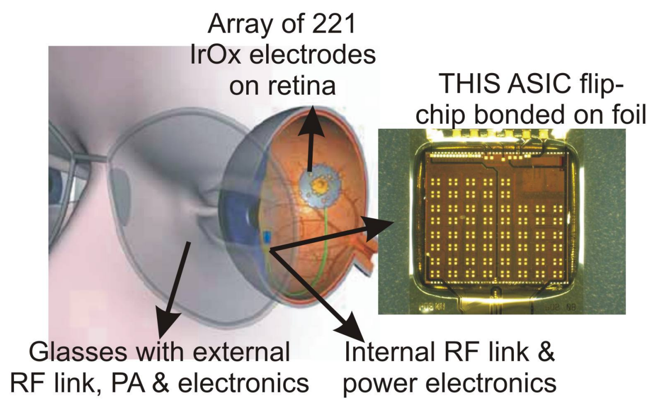

Figure 8.1.1: Epiretinal stimulator system.

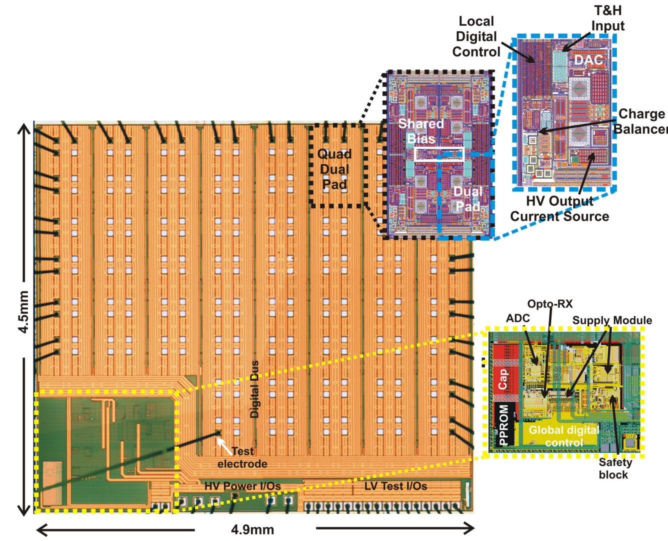

Figure 8.1.2: Chip micrograph and layout of the 232-channel stimulator ASIC.

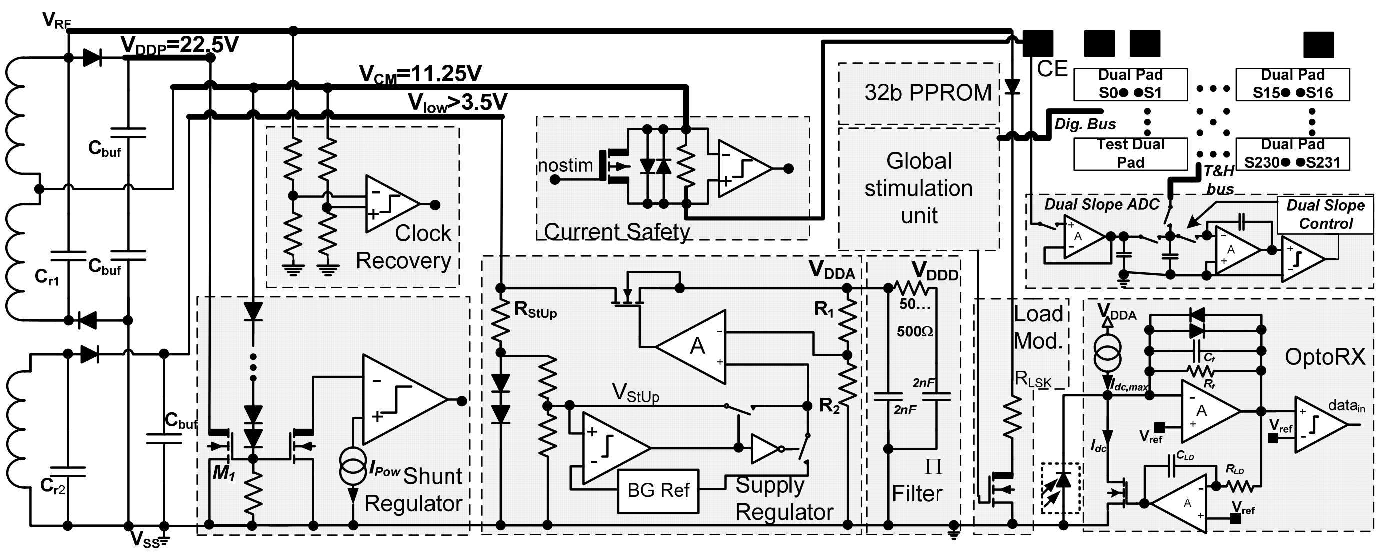

Figure 8.1.3: Illustration of global stimulator functions; for local functions see [2].

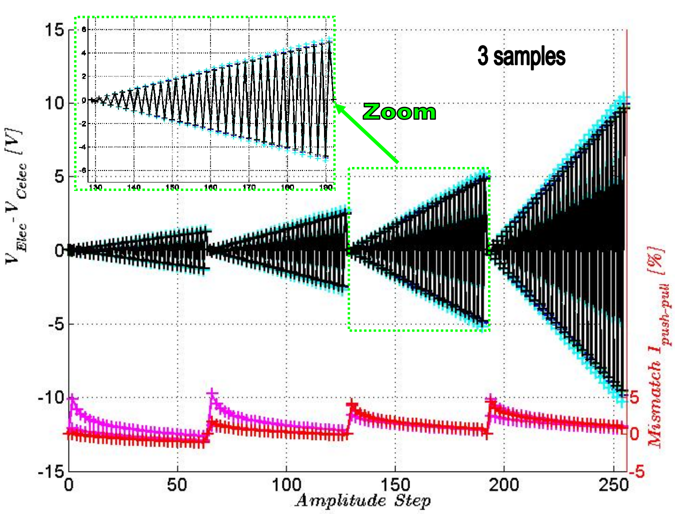

Figure 8.1.4: Push-pull electrode output voltage over 10kΩ and percentage current mismatch.

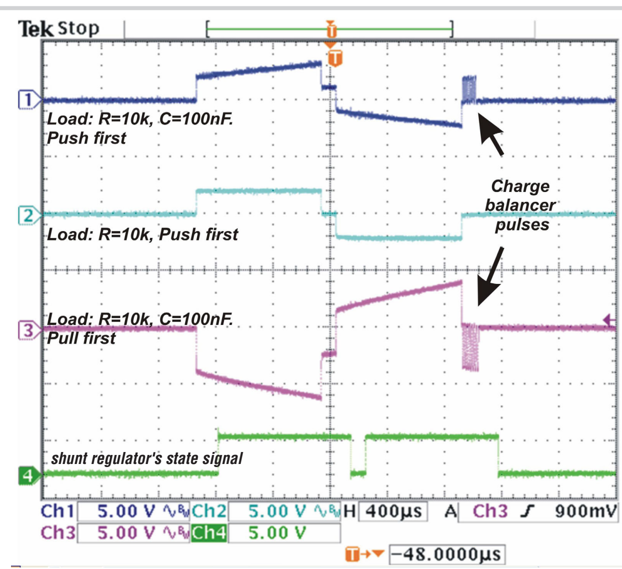

Figure 8.1.5: Exemplary output waveforms.

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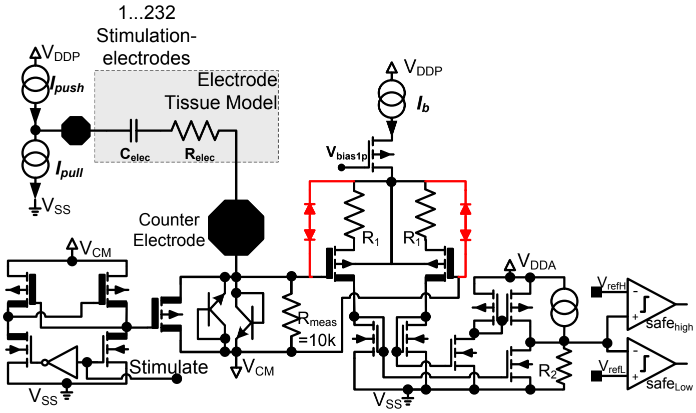

Figure 8.1.6: Schematic of the HV current safety circuit.

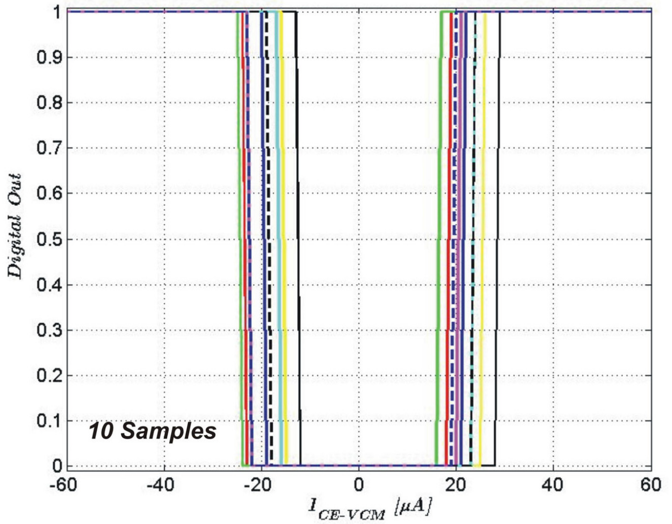

Figure 8.1.7: Digital output of safety block due to mismatch current between VCM and the counter electrode.